Remarks:

Applicants (hereinafter, Applicant) hereby request reconsideration of the application.

Applicant acknowledges the Examiner's confirmation of receipt of the claim for priority and certified copy of the priority application under 35 U.S.C. § 119(a)-(d).

In item 3 on page 2 of the above-identified Office action, the drawings have been objected to. The Examiner's suggested corrections are appreciated and have been made. More specifically, descriptive labels have been added to the boxes of Fig. 1.

In item 4 on page 2 of the above-identified Office action, the *abstract* has been objected to. The Examiner's suggested corrections are appreciated and Applicant has supplied a new *Abstract* on a separate page.

Claims 11-21 are now in the application. Claim 11 has been amended. No new matter is believed to be added.

In item 6 on page 3 of the Office action, claims 11-17 have been rejected as being fully anticipated by Chonan (U.S. Pat. No. 5,463,588) under 35 U.S.C. § 102.

In item 8 on page 4 of the Office action, claims 18, 19 and 21 have been rejected as being obvious over Chonan in view of Olgaard et al. (U.S. Pat. No.5,939,949) (hereinafter, "Olgaard") under 35 U.S.C. § 103.

In item 9 on page 6 of the Office action, claim 20 has been rejected as being obvious over Chonan in view of Olgaard and Tomassetti et al. (U.S. Pat. No.5,043,677) (hereinafter, "Tomassetti") under 35 U.S.C. § 103.

The rejections have been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. For support, see page 4, lines 19-20 and line 27 of the specification of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 11 calls for, inter alia, a controllable current source circuit, comprising:

*a first driver stage having a first controlled path containing a first transistor and a second driver stage having a second controlled path containing a second transistor, said first and*

*second controlled paths connected in series between said voltage supply terminal and said reference potential terminal; and*

*only said first driver stage switching on and off in dependence on an input signal, and said second driver stage being switched on and carrying a stabilized current.*

(Emphasis added.)

Accordingly, in the *present invention*, a controllable current source circuit and a phase locked loop equipped with such a circuit are disclosed. The current source circuit has a single switched driver stage for a switched actuation of the loop filter. A continuously switched-on driver stage is introduced into one of the paths of the current source circuit, so that a continuously weaker current is drawn by the loop filter.

In other words, the *present invention* includes a supply voltage terminal 12 and a reference potential terminal 13. See amended claim 11. A first driver stage contains a controlled path of a transistor (emitter-collector-path of transistor 17), and a second driver stage contains another controlled path of another transistor (collector-emitter-path of transistor 18). The controlled paths of transistors 17 and

18 are connected in series between the supply voltage terminal and the reference potential terminal. The series connection of transistors 17 and 18 is shown in current source circuit 7. See Fig. 2. The supply voltage connection 12 and the ground potential connection 13 are further discussed at page 4, lines 19-20 and at line 27 of the specification of the instant application.

The reference numerals corresponding to the above-features are presented solely for illustrative purposes. They are not intended to narrow the scope of the claims for any reason whatsoever.

The Chonan reference discloses a dynamic memory device having an internal power source circuit for generating an internal power voltage, which is smaller than an external power voltage applied to the device and supplied to an internal memory circuit as an operating voltage. The internal power source circuit includes a differential amplifier for stabilizing the internal power voltage in response to a reference voltage.

A current flowing through the differential amplifier is controlled so as to have a given first value during a standby mode, a second value larger than the first value during a data sensing operation and restoring (refreshing) operation of an active mode, and a third value larger than the first value,

but smaller than the second value during the other operation of the active mode.

Accordingly, the Chonan reference does not show first and second driver stages, each having a controlled path of a transistor, which is connected in series between a supply voltage terminal and a reference potential terminal. In Chonan, a first driver stage 12 and a second driver stage 22 each contain a controlled path (drain-source-path) of a transistor. See Chonan at Fig. 1. The controlled paths of transistors 12, 22 are connected to each other and form a series connection. The series connection of transistors 12, 22 is connected between the same supply potential terminal VCC (in contrast to the *present invention)*. Thus, Chonan's transistors are *not* connected between the supply potential terminal and the reference potential terminal.

Consequently, the circuit shown in Chonan is different from the circuit of the *present invention*. According to the *present invention*, the transistor 18 constantly drains a current (which is received at terminal 8) to the reference potential terminal 13. The transistor 17 supplies (sources) a current to terminal 8, independent of its switching state. Hence, the circuit of the claimed invention can be used to drive a charge pump in a phase-locked loop.

In Chonan, the transistors 12, 22 are connected between the supply voltage terminal VCC and the output node VINT. The transistor 12 constantly supplies (sources) a current to the output node VINT. The transistor 22 supplies (sources) a current to the output node VINT depending on its switching state. In Chonan, the draining of a current is not disclosed. In other words, since the object of the Chonan reference is to provide a power source circuit to generate an internal power voltage VINT, it does not teach draining any current.

Applicant further points out that, since the current source circuit of claim 11 is neither taught nor suggested by the prior art, the phase-locked loop circuit of claim 18 (which includes the current source circuit of claim 11) is also not taught or suggested by the prior art.

Clearly, the references do not show "*a first driver stage having a first controlled path containing a first transistor and a second driver stage having a second controlled path containing a second transistor, said first and second controlled paths connected in series between said voltage supply terminal and said reference potential terminal; and only said first driver stage switching on and off in dependence on an input signal, and said second driver stage being switched on and carrying a stabilized current*", as

recited in claim 11 of the instant application (emphasis added). Thus, neither can the specific combination of the aforementioned limitations be shown. Claim 18 recites similar limitations.

In other words, the features including the limitations "*a first driver stage having a first controlled path containing a first transistor and a second driver stage having a second controlled path containing a second transistor, said first and second controlled paths connected in series between said voltage supply terminal and said reference potential terminal; and only said first driver stage switching on and off in dependence on an input signal, and said second driver stage being switched on and carrying a stabilized current*", as recited in claim 11, attain the present invention's objectives and are not taught or suggested by the references, whether taken alone or in any combination (emphasis added).

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 11 and 18. Claims 11 and 18 are, therefore, believed to be patentable over the art and since all of the dependent claims are ultimately dependent on claims 11 and 18, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 11-21 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, the Examiner is respectfully requested to telephone counsel so that, if possible, patentable language can be worked out.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicant

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VRP:cgm

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Claim 11 (amended). A controllable current source circuit, comprising:

an output;

a supply voltage [terminals] terminal and a reference potential terminal;

a first driver stage having a first controlled path containing a first transistor and a second driver [stages] stage having a second controlled path containing a second transistor, said first and second controlled paths connected in series between said voltage supply terminal [terminals] and said reference potential terminal [and having a mutual junction point connected to said output]; and

[wherein] only said first driver stage [switches] switching on and off in dependence on an input signal, and said second driver stage [is] being switched on and [carries] carrying a stabilized current.